Preliminary Product Specification

Module name: C0201QILK-C

Issue date: 2008/06/24

Version: 1.5

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	**ENG Division**	**QA Dept**

Note:

1. The information contained herein may be change without prior notice. It is therefore advisable to contact Chi MEI ELCorp before designed your product based on this specification.

Reversion History

Version	Date	Page	Description
Ver.1.0	2008/03/11	All	Preliminary specification was first issued
Ver.1.1	2008/03/12	Page17	Modify the connector in the drawing
Ver.1.2	2008/06/04	Page3	Modify the pixel pitch size
		Page17	Modify the Panel drawing
		Page18	Add Reliability Test
		Page19	Add the Package drawing
Ver1.3	2008/06/19	Page12	Modify Electro-Optical Characteristic table
		Page13	Modify Gamma Register Setting
Ver1.4	2008/06/20	Page12	Modify IC Initial Register Setting
Ver1.5	2008/06/24	Page19	Add RA condition
			Modify Low Temp. Operation

1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

2. General Description:

- Driving Mode: Active Matrix.
- Color Mode: Full Color (262K color)
- Driver IC: S6E63D6, COG Assembly
- Interface:

1. MPU i80-system 18-/16-/9-/8-bit bus interface
2. MPU i68-system 18-/16-/9-/8-bit bus interface
3. Serial data transfer interface

- Application: Cell phone etc..
- RoHS Compatible

3. Mechanical Data:

No.	Items	Specification	Unit
1	**Diagonal Size**	2.0"	Inch
2	**Resolution**	176 xRGBx220	
3	**Pixel Pitch**	0.18×0.18	mm
4	**Active Area**	31.68×39.6	mm
5	**Outline Area(M/F)**	37.3×50.25	mm
6	**Thickness**	1.60 (Typ)	mm
7	**Weight**	9.2	g

4. Absolute Maximum ratings:

(VSS=0V)

Item	Symbol	Unit	Value	Note
Power supply voltage 1	VDD3	V	-0.3 ~ + 5.0	
Power supply voltage 2	VCI	V	-0.3 ~ + 5.0	
Input Voltage range	Vin	V	-0.3 ~ VDD+0.5	
Operating temperature	Topr	C	-20 ~ + 60	
Storage temperature	Tstg	C	-40~ + 85	

Notes:

(1) Absolute maximum rating is the limit value. When the IC is exposed operation environment beyond this range, the IC do not assure operations and may be damaged permanently, not be able to be recovered.

(2) Absolute maximum rating is guaranteed only when our company's package used.

5. Electrical Characteristic:

5.1 DC Characteristic

(Ta = -40℃ ~ 85℃, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	3.0	-	8.0	V	
	VGL	-	-8.0	-	-3.0	V	
	VINT	-	-4.0	-	-1.0	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	fosc	Frame frequency = 60Hz Display line = 320 line	1161.1	1290.2	1419.3	kHz	
1st booster input voltage	VCI1	-	2.1	-	2.75	V	
1st booster output voltage	VLOUT1	Without load	+4.6	-	+5.5	V	
1st booster output efficiency	VLOUT1	$I_{_VLOUT1_LOAD}$ = 2.3mA	90	95	-	%	
2nd booster output voltage	VLOUT2	Without load		7.8		V	
2nd booster output efficiency	VLOUT2	$I_{_VLOUT2_LOAD}$ = 0.1mA	90	93	-	%	
3rd booster output voltage	VLOUT3	Without load	-	-10.6	-	V	
3rd booster output efficiency	VLOUT3	$I_{_VLOUT3_LOAD}$ = 0.1mA	90	93	-	%	
Source Output voltage deviation (channel to channel)	-	-	-	±5	-	mV	
Source Output voltage difference (nearest channel)	-	20 Gray Pattern	-	5	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	±15	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	±15	-	mV	
Source driver output voltage range	Vso	-	0.3	-	4.2	V	
Driving voltage	dVGH	voltage deviation	-	-	300	mV	
	dVGL	voltage deviation	-	-	300	mV	
Current consumption during normal operation	IVDD3	No load, Ta = 25 °C	-	1.0	5.0	uA	*1
	IVCI		-	3.5	4.0	mA	
Stand by mode current	IVDD3	Ta = 25 °C	-	0.1	5.0	uA	
	IVCI		-	10	20	uA	

Note
1. VDD3=1.8V, VCI=2.8V, fosc=1290.2KHz (320 display line), NL[5:0]=" 10_1000", SAP[2:0]="101", DC22[2:0]="100", DC12[2:0]="010" , BT[1:0]=10, VC[3:0]="1000", VGH[4:0]="10100", VGL[4:0]="10100", VINT[3:0]="0101"

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power Supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply Voltage	1.65	1.8	3.3	V	
Logic High level input voltage	V_{IH}		0.7*VDD3		VDD3	V	
Logic Low level input voltage	V_{IL}		0.0		0.3*VDD3	V	
Logic High level output voltage	V_{OH}	IOUT = -1mA	0.8*VDD3		VDD3	V	
Logic Low level output voltage	V_{OL}	IOUT = +1mA	0.0		0.2*VDD3	V	
Analog High level output voltage	EL_ON_{OH}	8uA	1.8		VCI	V	
Analog Low level output voltage	EL_ON_{OL}	8uA	0		0.3	V	

Table 81. DC Characteristics 3

(VDD3 = 1.65~3.3V, VCI = 2.5~3.3V, Ta = 25℃)

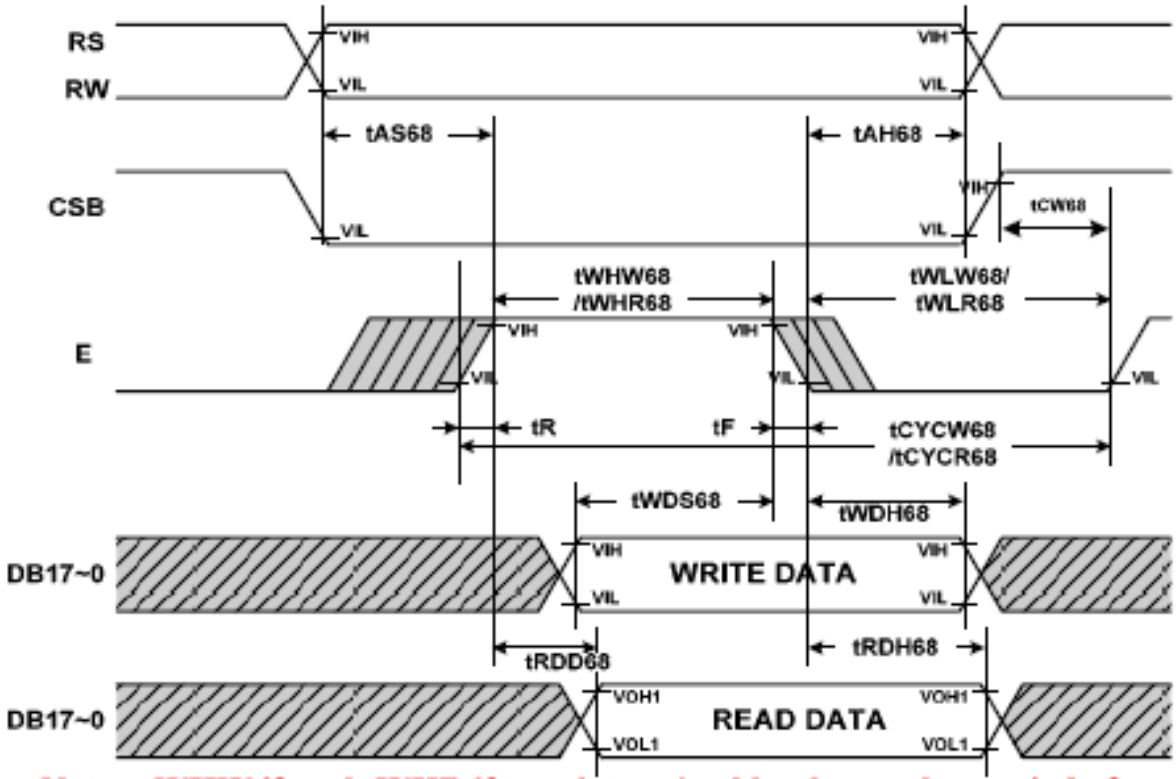
Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
VREG1OUT		.	4.185	4.2	4.215	V	

5.2 AC Characteristic

5.2.1 CPU interface M68

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW68	85	-	ns
	Read	tCYCR68	500	-	ns
Pulse rise / fall time		tR, tF	-	15	ns
Pulse width low	Write	tWLW68	27.5	-	ns
	Read	tWLR68	250	-	ns
Pulse width high	Write	tWHW68	27.5	-	ns
	Read	tWHR68	250	-	ns
RS,RW to CSB, E setup time		tAS68	10	-	ns
RS,RW to CSB, E hold time		tAH68	2	-	ns
CSB to E time		tCW68	15	-	ns
Write data setup time		tWDS68	40	-	ns
Write data hold time		tWDH68	15	-	ns
Read data delay time		tRDD68	-	200	ns
Read data hold time		tRDH68	5	-	ns

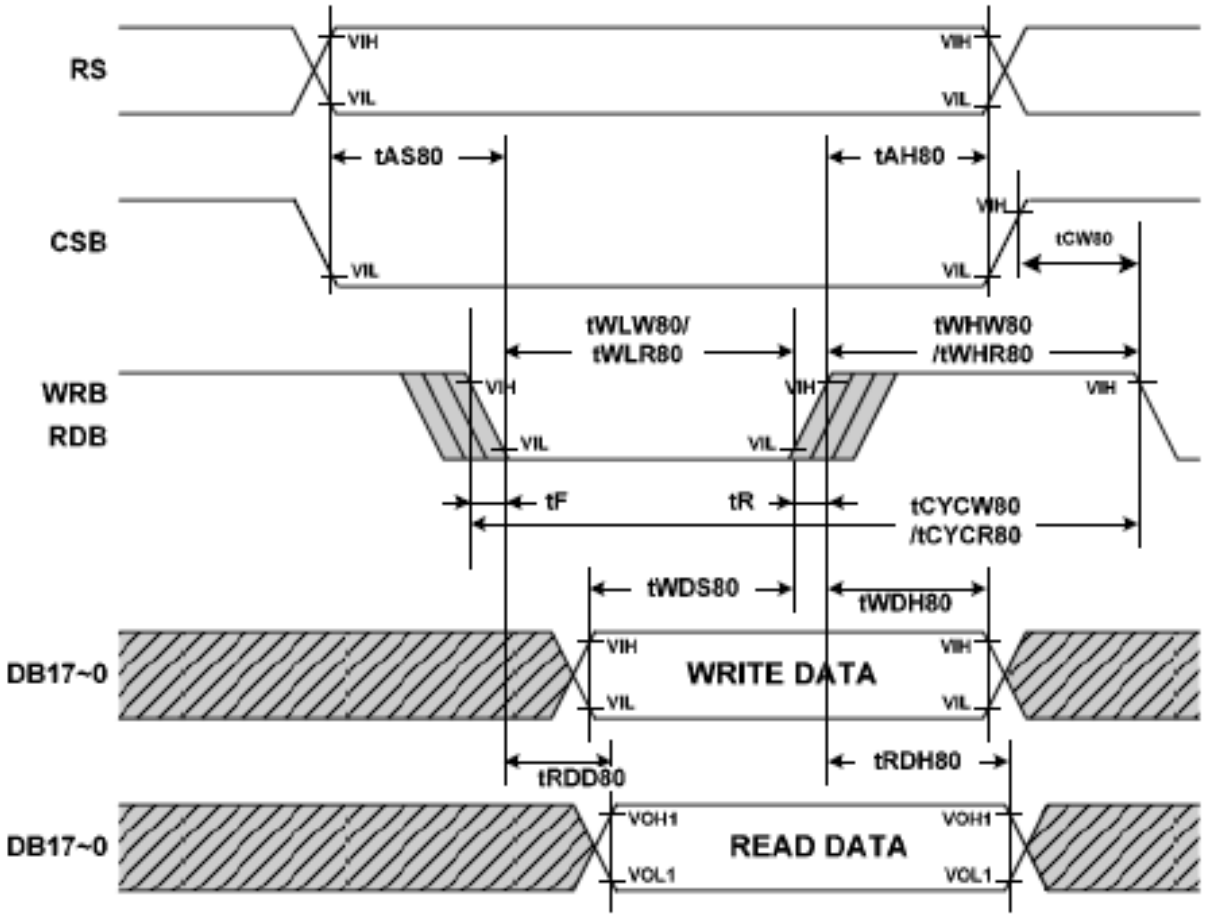


Note : tWHW68 and tWHR68 are determined by the overlap period of low CSB and high E

5.2.2 CPU interface M80

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW80	85	-	ns
	Read	tCYCR80	500	-	ns
Pulse rise / fall time		tR, tF	-	15	ns
Pulse width low	Write	tWLW80	27.5	-	ns
	Read	tWLR80	250	-	ns
Pulse width high	Write	tWHW80	27.5	-	ns
	Read	tWHR80	250	-	ns
RS to CSB, WRB(RDB) setup time		tAS80	10	-	ns
RS to CSB, WRB(RDB) hold time		tAH80	2	-	ns
CSB to WRB(RDB) time		tCW80	15	-	ns
Write data setup time		tWDS80	40	-	ns
Write data hold time		tWDH80	15	-	ns
Read data delay time		tRDD80	-	200	ns
Read data hold time		tRDH80	5	-	ns



Note : tWLW80 and tWLR80 are determined by the overlap period of low CSB and low WRB or low CSB and low RDB

Image Data format for 18bit CPU interface (262k color)

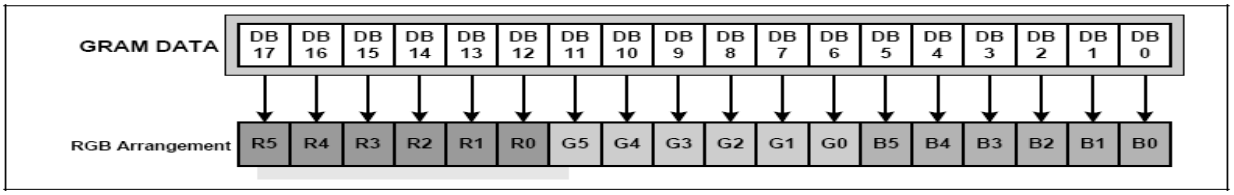


Image Data format for 16bit CPU interface (65k color)

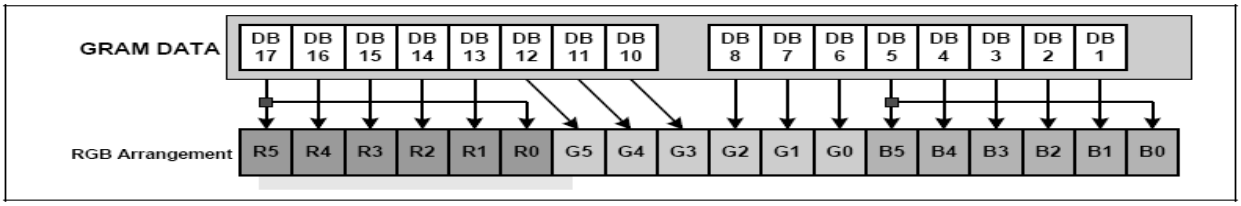


Image Data format for 9bit CPU interface (262k color)

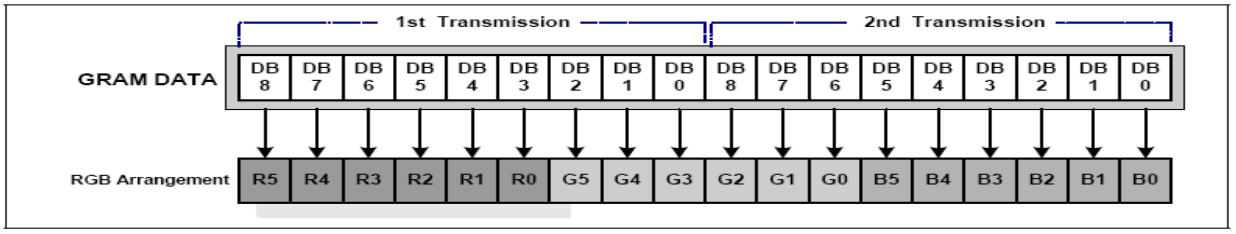
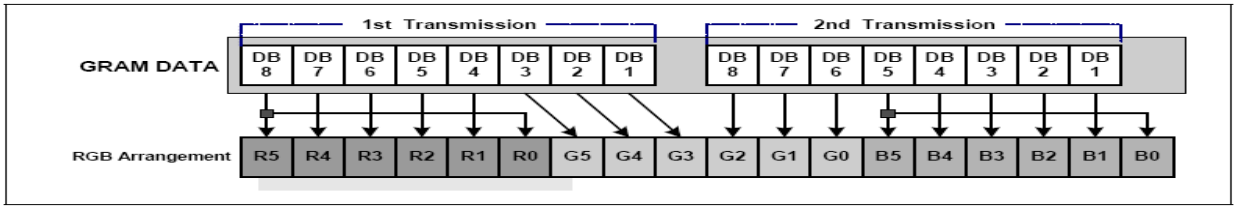


Image Data format for 8bit CPU interface (65K color)

Case 1:



Case 2:

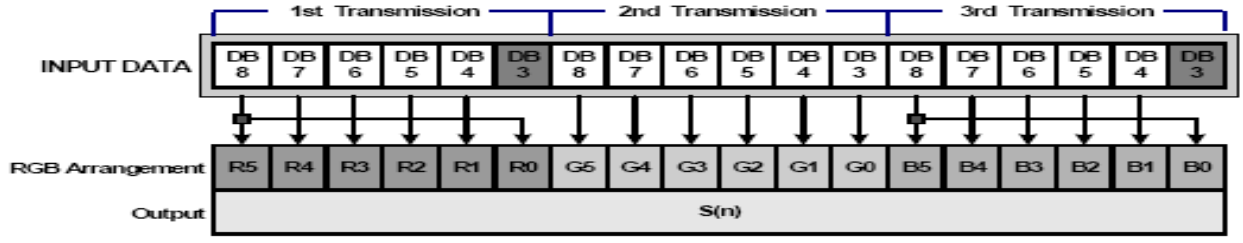
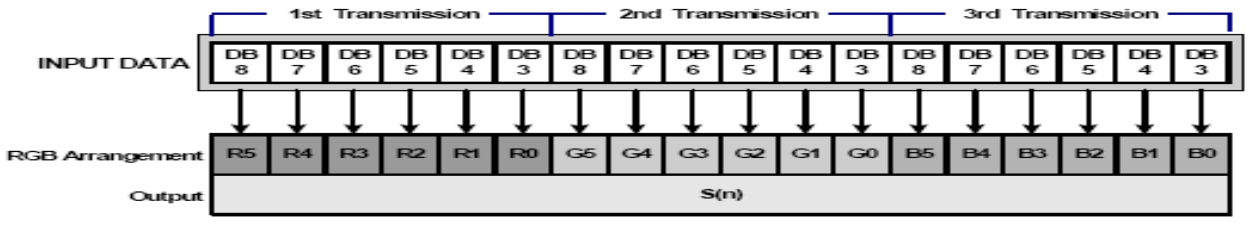


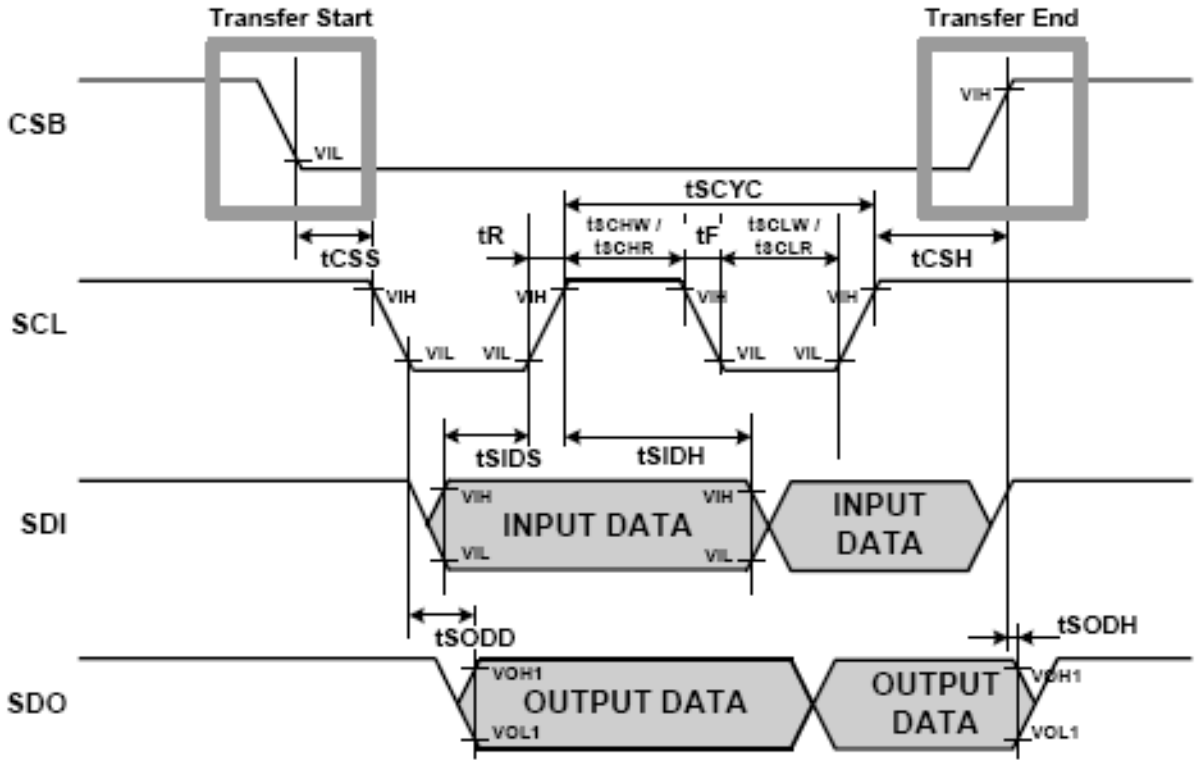
Image Data format for 8bit CPU interface (262K color)

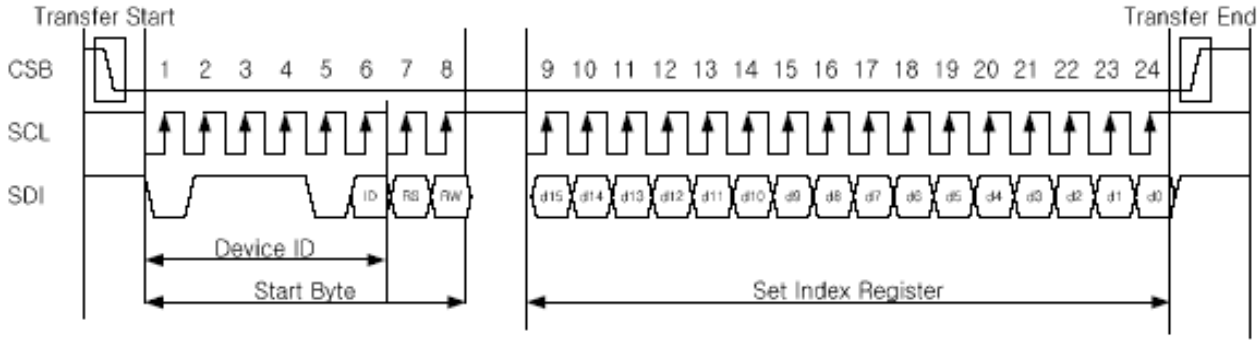


5.2.3 SPI

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tSCYC	130	-	ns
Serial clock read cycle time	tSCYC	250	-	ns
Serial clock rise / fall time	tR, tF	-	15	ns
Pulse width high for write	tSCHW	50	-	ns
Pulse width high for read	tSCHR	110	-	ns
Pulse width low for write	tSCLW	50	-	ns
Pulse width low for read	tSCLR	110	-	ns
Chip select setup time	tCSS	20	-	ns
Chip select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns





(Note) RS=”0” : Index data

RS=”1” : Instruction data

6. Electro-Optical Characteristic:

Items	Symbol	Min	Typ.	Max	Unit	Remark
Operating Luminance	L	150	175	200	Cd/m^2	(1)(5)
Power Consumption	Pon	-	150	200	mW	30% pixels on (1)
Max. Current	Icc	-	-	66	mA	(1)
Response Time	Tres	-	-	50	us	(2)
CIEx (White)	Wx	0.26	0.31	0.36	-	(5)
CIEy(White)	Wy	0.28	0.33	0.38	-	(5)
CIEx (Red)	Rx	0.62	0.66	0.70		(5)
CIEy(Red)	Ry	0.30	0.34	0.38		(5)
CIEx (Green)	Gx	0.25	0.29	0.33		(5)
CIEy(Green)	Gy	0.61	0.65	0.69		(5)
CIEx (Blue)	Bx	0.11	0.15	0.19		(5)
CIEy(Blue)	By	0.12	0.16	0.20		(5)
Viewing Angle	VA	160	170	-	Degree	(3)
Contrast	CR	5000:1	10000:1			(4)
Operation Lifetime	LTop	20000			Hrs	(1)(6)

Note:

Measuring surrounding: dark room

Surrounding temperature: 25°C

IOVCC = 1.65V ~ 3.3V

1. Test condition:

a. AR_VDD= 4.6V+/- 0.03V, AR_VSS= -4.4V+/- 0.03V

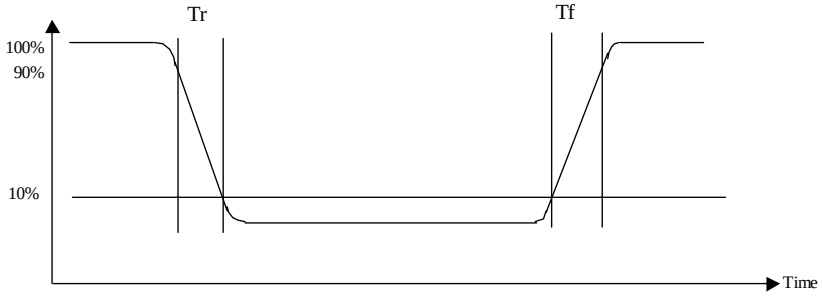
b. IC Initial Register Setting:

R01: 0x881C // Set scan line
R02: 0x0000
R03: 0x0030 // 16bit mode
R10: 0x0000 // IC stand by off
R18: 0x0028 // Frame Rate=80Hz
RF8: 0x000F // VGH=+5V
RF9: 0x0019 // VGL=-7V
R05: 0x0001 // Display On
R35: 0x0000 // window display
R36: 0x00DB // window display
R37: 0x20CF // window display
R20: 0x0020 // window display
R21: 0x0000 // window display

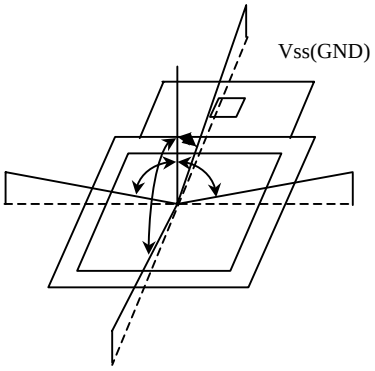
Gamma Register Setting:

R70: 0x3480
R71: 0x3900
R72: 0x3C80
R73: 0x291F
R74: 0x2119
R75: 0x3221
R76: 0x211A
R77: 0x2C22
R78: 0x271D

2.response Time test condition



3.Viewing angle test condition:



Viewing Angle= CR>10

ϕ =270°

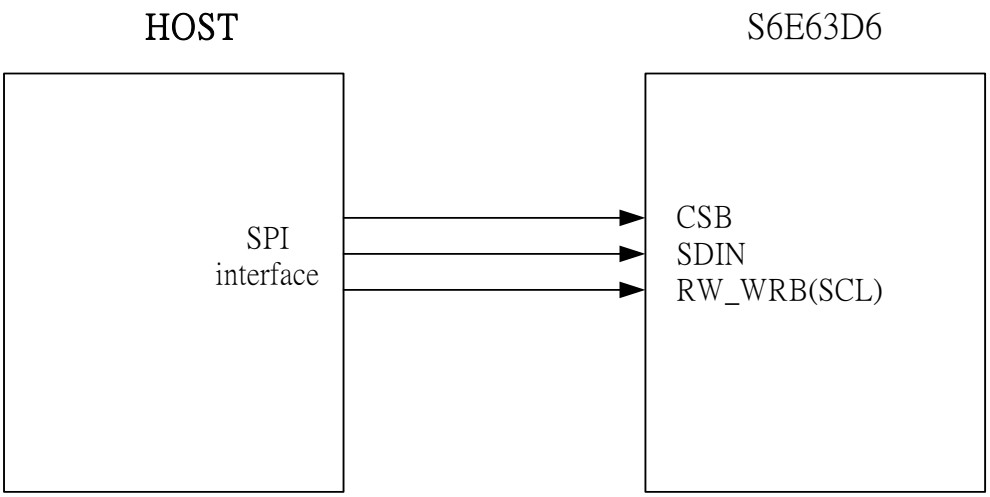
4.Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5.Optical tester: CA210

6. Brightness of 30% power consumption. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

7. System Diagram:



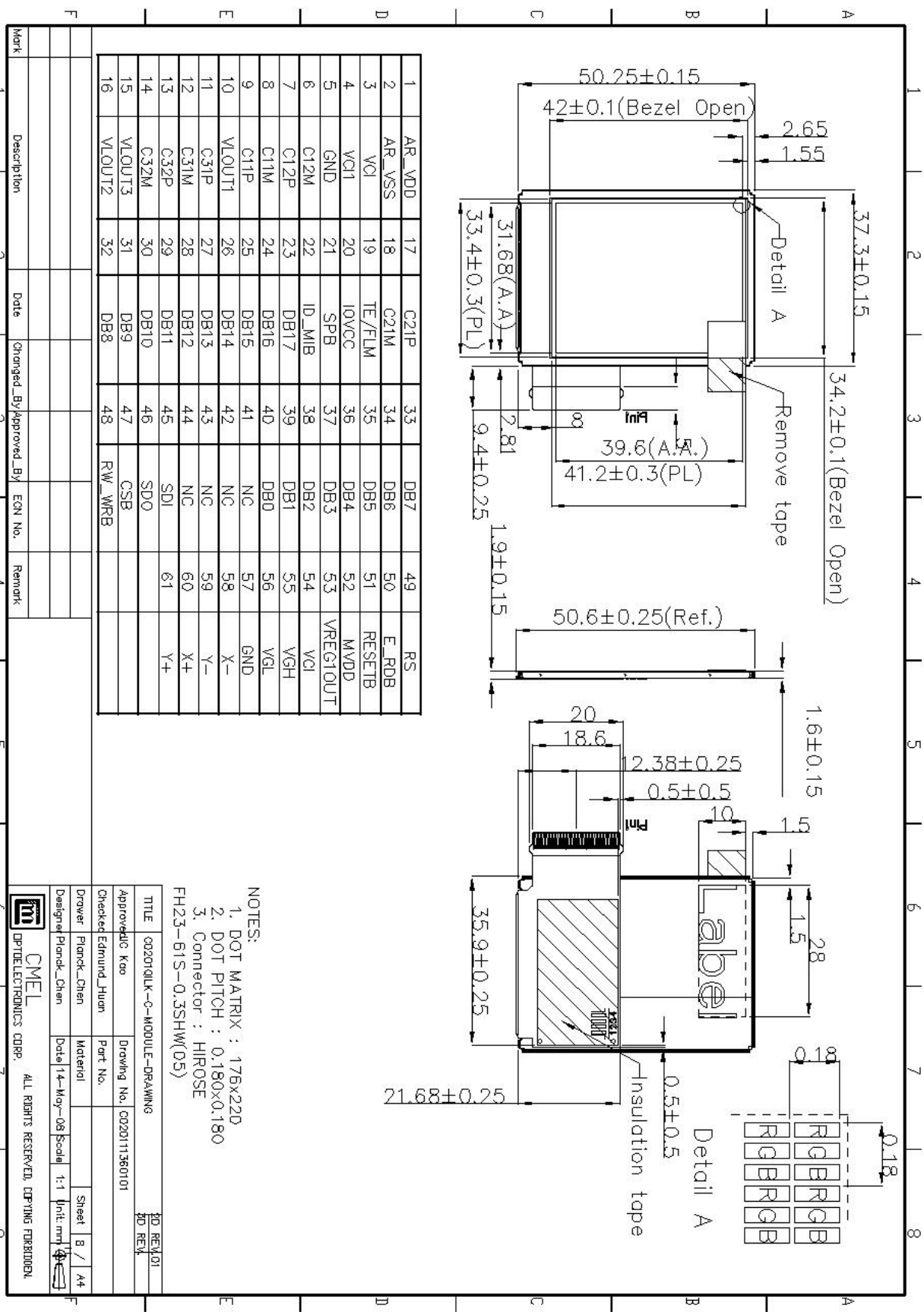
8. Pin Assignment:

PIN	Symbol	I/O	Description	Remarks
1	AR_VDD	I	Positive voltage for OLED	
2	AR_VSS	I	Nagative voltage for OLED	
3	VCI	I	Power supply for analog circuit(2.5v~3.3v)	
4	VCI1	O	A reference voltage for 1st booster r(connect a 1u/10v capacitance to gnd)	
5	GND	I	Ground	
6	C12M	I	External capacitance connect pin between C12M and C12P (1u/10V)	
7	C12P	I		
8	C11M	I	External capacitance connect pin between C11M and C11P (1u/10V)	
9	C11P	I		
10	VLOUT1	O	1st booster output pin. (1u/10V)	
11	C31P	I	External capacitance connect pin between C31M and C31P (1u/10V)	
12	C31M	I		
13	C32P	I	External capacitance connect pin between C32M and C32P (1u/10V)	
14	C32M	I		
15	VLOUT3	O	3rd booster output pin. (1u/16V)	
16	VLOUT2	O	2nd booster output pin. (1u/16V)	
17	C21P	I	External capacitance connect pin between C21M and C21P. (1u/10V)	
18	C21M	I		
19	FLM	O	Tearing effect output signal. In normal operation, leave this pad open.	
20	IOVCC	I	I/O power supply	
21	SPB	I	Select the CPU interface mode. (0=parallel interface 1=serial interface)	
22	ID_MIB	I	Select the CPU type (0=intel 80x-system 1=motorola 68x-system)	
23	DB17	I/O	BI-directional data bus. When CPU I/F, 18-bit interface : DB 17-0 16-bit interface : DB 17-10 , DB 8-1 9-bit interface : DB 8-0 8-bit interface : DB 8-1 When RGB I/F 18-bit interface : DB 17-0 18-bit interface : DB 17-0 16-bit interface : DB 17-10, DB 8-1 6-bit interface : DB 8-3 Fix unused pin to the VSS level	
24	DB16	I/O		
25	DB15	I/O		
26	DB14	I/O		
27	DB13	I/O		
28	DB12	I/O		
29	DB11	I/O		
30	DB10	I/O		
31	DB9	I/O		
32	DB8	I/O		
33	DB7	I/O		

34	DB6	I/O		
35	DB5	I/O		
36	DB4	I/O		
37	DB3	I/O		
38	DB2	I/O		
39	DB1	I/O		
40	DB0	I/O		
41	NC			
42	NC			
43	NC			
44	NC			
45	SDI	I	For a serial peripheral interface(SPI), input data is fetched at the rising edge of the SCL signal, Fix SDI pin at VSS level if the pin is not used.	
46	SDO	I	For a serial peripheral interface (SPI), serves as the serial data olutput pin(SDO), Successive bits are output at the falling edge of the SCL signal.	
47	CSB	I	Chip select signal input pin. 0= driver IC is selected and can be accessed. 1= driver IC is not selected and cannot be accessed.	
48	RW_WRB	I	Pin function / CPU type / Pin description RW / 68-system / Read/Write operation selection pin 0=write 1=read WRB / 80_system / Write strobe signal.(Input pin) Data is fetched at the rising edge. SCL / SPI / The synchronous clock signal	
49	RS	I	Register select pin. 0=Index/status, 1=instruction parameter, GRAM data Must be fixed at VDD3 level when not used.	
50	E_RDB	I	Pin Function / CPU type / Pin description E / 68-system / Read/Writeoperation enable pin RDB / 80_system / Read strobe signal. Read out data at the low level When SPI mode is selected , fix this pin at VDD3 levle	
51	RESETB	I	Reset pin initializes the IC when low. Should be reset after power-on.	
52	MVDD	O	Internal power for RAM. Connect a capacitance to gnd. Connect a capacitance(1u/10v) to gnd.	
53	VREG1OUT	O	A reference level for the grayscale voltage. Connect a capacitance(1u/10v) to gnd.	
54	VCI	I	Power supply for analog circuit(2.5v~3.3v)	
55	VGH	O	The positive voltage used in the gate driver. Connect a capacitance(1u/10v) to gnd.	
56	VGL	O	The negative voltage used in the gate driver. Connect a capacitance(1u/10v) to gnd.	
57	GND		Ground	
58	X-		For touch screen	

59	Y-		For touch screen	
60	X+		For touch screen	
61	Y+		For touch screen	

9. External Dimension:



1	AR_VDD	17	C21P	33	DB7	49	RS
2	AR_VSS	18	C21M	34	DB6	50	E_RDB
3	VCI	19	TE/FLM	35	DB5	51	RESETB
4	VCI1	20	IOVCC	36	DB4	52	MVDD
5	GND	21	SPB	37	DB3	53	VREG1OUT
6	C12M	22	ID_MIB	38	DB2	54	VCI
7	C12P	23	DB17	39	DB1	55	VGH
8	C11M	24	DB16	40	DB0	56	VGL
9	C11P	25	DB15	41	NC	57	GND
10	VLOUT1	26	DB14	42	NC	58	X−
11	C31P	27	DB13	43	NC	59	Y−
12	C31M	28	DB12	44	NC	60	X+
13	C32P	29	DB11	45	SDI	61	Y+
14	C32M	30	DB10	46	SDO		
15	VLOUT3	31	DB9	47	CSB		
16	VLOUT2	32	DB8	48	RW_WRB		

NOTES:
1. DOT MATRIX : 176x220
2. DOT PITCH : 0.180x0.180
3. Connector : HIROSE FH23-61S-0.3SHW(05)

Mark	Description	Date	Changed_By/Approved_By	ECN No.	Remark

TITLE	G020161LK-C-MODULE-DRAWING
Approved	Eric Kao
Checked	Edmund_Huan
Drawer	Planck_Chen
Designer	Planck_Chen
ID REV	ID REV:01
Drawing No.	C020111360101
Part No.	
Material	
Date	14-May-08
Scale	1:1
Unit: mm	Sheet B / A4

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10. Reliability Test:

No.	Items	Specification
1	High Temp. Storage	85°C, 240hrs
2	Low Temp. Storage	-40°C, 240hrs
3	High Temp. Operation	70°C, 240hrs
4	Low Temp. Operation	-40°C, 240hrs
5	High Temp / Humidity Storage	85°C, 85%RH, 240hrs
6	High Temp / Humidity Operation	60°C, 90%RH, 240hrs
7	Thermal shock	-40°C ~85°C (-40°C /30min; transit/3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles
8	Vibration	Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z
9	Drop	Height: Follow ISTA spec. Sequence : 1 angle、3 edges and 6 faces Cycles: 1
10	ESD	Air discharge model, ±8kV, 10 times

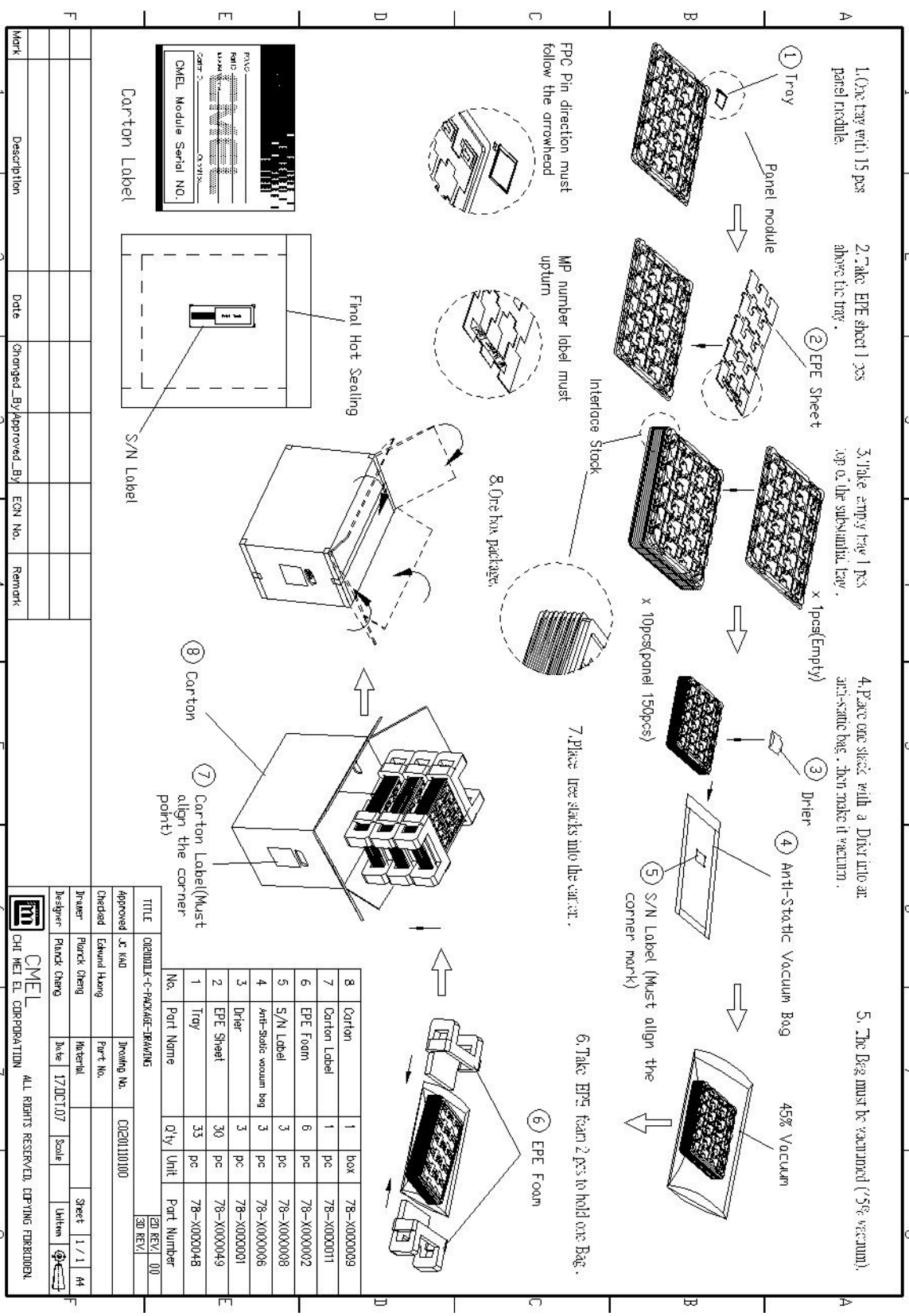
Test and measurement conditions

- All measurements shall not be started until the specimens attain to temperature stability.
- The degradation of Polarizer is ignored for item 1, 5 & 6.
- The test pattern at operating condition is 30%P.C. alternating pictures.

Evaluation Criteria

- No damage to glass or encapsulation
- No drastic change to display
- Defects / Mura follow product specification
- Luminance: Within +/-50% of initial value
- Current consumption: within +/-50% of initial value

11. Package:


1.One tray with 15 pcs panel module.
2.Take EPE sheet 1 pcs above the tray.
3.Take empty tray 1 pcs up to the subsumila tray.
4.Pack one sheet with a Drier into an anti-static bag, then make it vacuum.
5. The Bag must be vacuumed (75% vacuum).
① Tray
Panel module
② EPE Sheet
× 1pcs(Empty)
③ Drier
④ Anti-Static Vacuum Bag
45% Vacuum
Interlace Stock
× 10pcs(panel 150pcs)
⑤ S/N Label (Must align the corner mark)
6.Take EPE foam 2 pcs to hold one Bag.
⑥ EPE Foam
7.Place tray stacks into the carton.
8.One box package.
⑦ Carton Label(Must align the corner point)
⑧ Carton
Final Hot Sealing
S/N Label
MP number label must upturn
FPC Pin direction must follow the arrowhead
Carton Label
CMEL Module Serial NO.
Mark
Description
Date
Changed_By
Approved_By
ECN No.
Remark
TITLE
CQ20010LK-C-PACKAGE-DRAWING
Approved
JC KAO
Drawing No.
CQ20110100
Checked
Edmund Huang
Part No.
Drawer
Phorck Cheng
Material
Designer
Phorck Cheng
Date
17.OCT.07
Scale
Sheet
1 / 1
A4
Unit:mm
CMEL
CHI MEI EL CORPORATION
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2D REV. 00
3D REV.
No. Part Name Q'ty Unit Part Number
8 Carton 1 box 78-XXXX009
7 Carton Label 1 pc 78-XXXX011
6 EPE Foam 6 pc 78-XXXX002
5 S/N Label 3 pc 78-XXXX008
4 Anti-Static vacuum bag 3 pc 78-XXXX006
3 Drier 3 pc 78-XXXX001
2 EPE Sheet 30 pc 78-XXXX049
1 Tray 33 pc 78-XXXX048